Binary dump of the 82S123A (74S188) PROM contents

IC1: address	progr. Byte	6502 prozessor selected address space	Control function description
0 1	61 61	0x0xxx	Simulate an external address of 0x2xxx
2	43	0x80xx, 0x82xx, 0x84xx, ...	Simulate an external address of 0xA0xx, 0xA2xx, ..., enable the internal ROM (range 0x2000 to 0x2fff), switch the address bits A[0..3] to the internal AL address bus, switch the internal 4-Bit register output to the internal AH address bus and store the current AL address bus value (A[0..3])
3	107	0x81xx, 0x83xx, 0x85xx, ...	Simulate an external address of 0xA1xx, 0xA3xx, ..., enable the internal ROM (range 0x2000 to 0x2fff), switch the address bits A[4..7] to the internal AL address bus, switch the internal 4-Bit register output to the internal AH address bus and store the current AL address bus value (A[4..7])
4 5	61 61	0x4xxx	Simulate an external address of 0x6xxx
6 7	60 60	0xCxxx	
8 9	61 61	0x2xxx	
10 11	53 53	0xAxxx	Enable the internal RAM (range 0x0000 to 0x0fff)
12 13	61 61	0x6xxx	
14 15	13 13	0xExxx	Enable the internal ROM (range 0x0000 to 0x0fff)
16 17	61 61	0x1xxx	Simulate an external address of 0x3xxx
18 19	45 45	0x9xxx	Simulate an external address of 0xBxxx and enable the internal ROM (range 0x3000 to 0x3fff),
20 21	61 61	0x5xxx	Simulate an external address of 0x7xxx
22 23	60 60	0xDxxx	
24 25	61 61	0x3xxx	
26 27	53 53	0xBxxx	Enable the internal RAM (range 0x1000 to 0x1fff)
28 29	61 61	0x7xxx	
30	13	0xF0xx, 0xF2xx, 0xF4xx, ...	Enable the internal ROM (range 0x1000 to 0x1fff)
31	141	0xF1xx, 0xF3xx, 0xF5xx, ...	Enable the internal ROM (range 0x1000 to 0x1fff) and store the values of the address lines A1 and A2 to the internal clock mode Flip-Flops

Function oriented listing of the 82S123A (74S188) PROM contents

Line label	A15	A14	A13	A12	A8	6502 prozessor selected address space	programmed byte (dez)	FETCH-2MHZ-MODE	A13-EXT (6502 adaptor)	O1&O8-Function	ROM-/OE	ROM-BANKSEL	RAM-/CS1	O4..O6-Function	SELECT-A[0..3|4..7]->AL	/EN-AL->AH (Latched)	/EN-A[4..7]->AH	O2-, O3-, O7-Function
IC1-Addr	A1	A2	A3	A4	A0			O8	O1		O5	O6	O4		O7	O3	O2	
0	0	0	0	0	0	0x0xxx	61	0	1	Selected ext. addr.:	1	1	1		0	1	0	
1	0	0	0	0	1		61	0	1	0x2xxx	1	1	1		0	1	0	
16	0	0	0	1	0	0x1xxx	61	0	1	A-EXT: 0x3xxx	1	1	1		0	1	0	
17	0	0	0	1	1		61	0	1		1	1	1		0	1	0	
8	0	0	1	0	0	0x2xxx	61	0	1		1	1	1		0	1	0	
9	0	0	1	0	1		61	0	1		1	1	1		0	1	0	
24	0	0	1	1	0	0x3xxx	61	0	1		1	1	1		0	1	0	
25	0	0	1	1	1		61	0	1		1	1	1		0	1	0	AL=A[0..3]
4	0	1	0	0	0	0x4xxx	61	0	1	A-EXT: 0x6xxx	1	1	1		0	1	0	AH=A[4..7]
5	0	1	0	0	1		61	0	1		1	1	1		0	1	0	
20	0	1	0	1	0	0x5xxx	61	0	1	A-EXT: 0x7xxx	1	1	1		0	1	0	
21	0	1	0	1	1		61	0	1		1	1	1		0	1	0	
12	0	1	1	0	0	0x6xxx	61	0	1		1	1	1		0	1	0	
13	0	1	1	0	1		61	0	1		1	1	1		0	1	0	
28	0	1	1	1	0	0x7xxx	61	0	1		1	1	1		0	1	0	
29	0	1	1	1	1		61	0	1		1	1	1		0	1	0	
2	1	0	0	0	0	0x80xx, 0x82xx, 0x84xx, ...	43	0	1	A-EXT: 0xAxxx	0	1	1	Enable HI-ROM	0	0	1	AL=A[0..3], AH=AL(prev.)
3	1	0	0	0	1	0x81xx, 0x83xx, 0x85xx, ...	107	0	1		0	1	1	(GCR-Tables)	1	0	1	AL=A[4..7], AH=AL(prev.)
18	1	0	0	1	0	0x9xxx	45	0	1	A-EXT: 0xBxxx	0	1	1	Enable HI-ROM	0	1	0	AL=A[0..3]
19	1	0	0	1	1		45	0	1		0	1	1	(Prof-DOS-Ext.)	0	1	0	AH=A[4..7]
10	1	0	1	0	0	0xAxxx	53	0	1		1	1	0		0	1	0	
11	1	0	1	0	1		53	0	1		1	1	0	Enable RAM	0	1	0	AL=A[0..3]
26	1	0	1	1	0	0xBxxx	53	0	1		1	1	0	(O4=0, O6=1)	0	1	0	AH=A[4..7]
27	1	0	1	1	1		53	0	1		1	1	0		0	1	0	
6	1	1	0	0	0	0xCxxx	60	0	0		1	1	1		0	1	0	
7	1	1	0	0	1		60	0	0		1	1	1		0	1	0	
22	1	1	0	1	0	0xDxxx	60	0	0		1	1	1		0	1	0	
23	1	1	0	1	1		60	0	0		1	1	1		0	1	0	AL=A[0..3]
14	1	1	1	0	0	0xExxx	13	0	1		0	0	1	Enable LO-ROM	0	1	0	AH=A[4..7]
15	1	1	1	0	1		13	0	1		0	0	1		0	1	0	
30	1	1	1	1	0	0xF0xx, 0xF2xx, 0xF4xx, ...	13	0	1		0	0	1	Enable LO-ROM	0	1	0	
31	1	1	1	1	1	0xF1xx, 0xF3xx, 0xF5xx, ...	141	1	1	Write clock mode	0	0	1	(Profess.-DOS)	0	1	0	